CLAIMS

[0062] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A pixel cell comprising:

a substrate;

a gate of a transistor formed at least partially below the surface of the substrate; and

a photo-conversion device formed adjacent to the gate, the photo-conversion device comprising a doped surface layer of a first conductivity type, and a doped region of a second conductivity type underlying the doped surface layer, wherein the doped surface layer is at least partially above a level of a bottom surface of the gate.

2. The pixel cell of claim 1, wherein the first and second conductivity types are p and n respectively.

3. The pixel cell of claim 1, wherein the photo-conversion device is a pinned photodiode.

4. The pixel cell of claim 1, wherein the gate is the gate of a transfer transistor.

5. The pixel cell of claim 1, wherein the gate is the gate of a reset transistor.

6. The pixel cell of claim 1, wherein the gate is the gate of a charge coupled device.

7. The pixel cell of claim 1, further comprising a sensing node adjacent to the gate and on an opposite side of the gate from the photo-conversion device.

8. The pixel cell of claim 7, wherein the sensing node is a floating diffusion region.

9. The pixel cell of claim 1, wherein the doped surface layer has a thickness within the range of approximately 200 to approximately 2000 Å.

10. The pixel cell of claim 1, wherein the implant dose of a dopant for the doped surface layer is within the range of approximately 1×10^{12} to approximately 3×10^{14} atoms per cm^2.

11. The pixel cell of claim 1, wherein the doped surface layer is at a level approximately between a level of a top surface of the gate and a level of the bottom surface of the gate.

12. The pixel cell of claim 1, further comprising a trench in the substrate, wherein the gate is at least partially in the trench.

13. The pixel cell of claim 12, wherein the trench has a depth within the range of approximately 500 to approximately 2500 Å.

14. The pixel cell of claim 1, wherein the gate comprises:

a conductive layer; and

insulating material, wherein the insulating material is on at least two lateral sides of the conductive layer.

15. The pixel cell of claim 14, wherein the insulating material on the two lateral sides of the gate has a thickness within the range of approximately 20 to approximately 100 Å thick.

16. The pixel cell of claim 14, wherein the doped surface layer is in contact with the insulating material.

17. The pixel cell of claim 1, wherein operation of the gate affects the doped surface layer at least partially through a sidewall of the gate.

18. The pixel cell of claim 1, wherein the gate is part of a CMOS imager.

19. The pixel cell of claim 1, wherein the gate is part of a charge coupled device imager.

20. A pixel cell comprising:

a substrate;

a trench in the substrate;

a gate of a transistor at least partially in the trench;

a photo-conversion device formed adjacent to the trench, the photo-conversion device comprising a doped layer of a first conductivity type below the surface of the substrate, and a doped region of a second conductivity type underlying the doped layer of a first conductivity type, wherein the doped surface layer is at least partially above a level of a bottom surface of the trench.

21. The pixel cell of claim 20, wherein the trench has a depth within the range of approximately 500 to approximately 2500 Å.

22. The pixel cell of claim 20, wherein the gate comprises:

a conductive layer; and

insulating material, wherein the insulating material is on at least two lateral sides of the conductive layer.

23. The pixel cell of claim 22, wherein the insulating material on the two lateral sides of the gate has a thickness within the range of approximately 20 to approximately 100 Å thick.

24. An imager system, comprising:

(i) a processor; and

(ii) an imager coupled to the processor, the imager comprising:

a substrate;

a pixel formed over the substrate, the pixel comprising:

a gate of a transistor formed at least partially below the surface of the substrate; and

a photo-conversion device formed adjacent to the gate, the photo-conversion device comprising a doped surface layer of a first conductivity type, and a doped region of a second conductivity type underlying the doped surface layer, wherein the doped surface layer is at least partially above a level of a bottom surface of the gate.

25. The system of claim 24, wherein the imager is a CMOS imager.

26. The system of claim 24, wherein the imager is a charge coupled device imager.

27. The system of claim 24, wherein the first and second conductivity types are p and n respectively.

28. The system of claim 24, wherein the photo-conversion device is a pinned photodiode.

29. The system of claim 24, wherein the gate is the gate of a transfer transistor.

30. The system of claim 24, wherein the gate is a transfer gate of a charge coupled device.

31. The system of claim 24, further comprising a sensing node adjacent to the gate and on an opposite side of the gate from the photo-conversion device.

32. The system of claim 31, wherein the sensing node is a floating diffusion region.

33. The system of claim 24, wherein the doped surface layer has a thickness within the range of approximately 200 to approximately 2000 Å.

34. The system of claim 24, wherein the doped surface layer is at a level approximately between a level of a top surface of the gate and a level of the bottom surface of the gate.

35. The system of claim 24, further comprising a trench formed in the substrate, wherein the gate is at least partially in the trench.

36. The system of claim 35, wherein the trench has a depth within the range of approximately 500 to approximately 2500 Å.

37. The system of claim 24, wherein operation of the gate affects the doped surface layer at least partially through a sidewall of the gate.

38. A method of forming a pixel cell, the method comprising:

providing a substrate;

forming a gate of a transistor at least partially below a surface of the substrate; and

forming a photo-conversion device adjacent to the gate, the act of forming the photo-conversion device comprising forming a doped surface layer of a first conductivity type, and forming a doped region of a second conductivity type underlying the doped surface region, wherein the act of forming the doped surface layer comprises forming the doped surface layer at least partially above a level of a bottom surface of the gate.

39. The method of claim 38, wherein the first and second conductivity types are p and n respectively.

40. The method of claim 38, wherein the act of forming the photo-conversion device comprises forming a pinned photodiode.

41. The method of claim 38, wherein the act of forming the gate comprises forming a gate of a transfer transistor.

42. The method of claim 38, wherein the act of forming the gate comprises forming a gate of a reset transistor.

43. The method of claim 38, wherein the act of forming the gate comprises forming a gate of a charge coupled device.

44. The method of claim 38, further comprising forming a sensing node adjacent to the gate and on a side of the gate opposite to the photo-conversion device.

45. The method of claim 44, wherein the act of forming the sensing node comprises forming a floating diffusion region.

46. The method of claim 38, wherein the doped surface layer is formed at a level approximately between a level of a top surface of the gate and a level of the bottom surface of the gate.

47. The method of claim 38, wherein the doped surface layer is formed having a thickness within the range of approximately 200 to approximately 2000 Å.

48. The method of claim 38, wherein the act of forming the doped surface layer comprises forming the doped surface layer having an implant dose of a dopant within the range of approximately 1×10^{12} to approximately 3×10^{14} atoms per cm^2.

49. The method of claim 38, further comprising forming a trench in the substrate prior to forming the gate, and wherein the act of forming the gate comprises forming the gate at least partially in the trench.

50. The method of claim 49, wherein the trench is formed having a depth within the range of approximately 500 to approximately 2500 Å.

51. The method of claim 38, wherein the act of forming the gate comprises:

forming a conductive layer; and

forming an insulating layer, such that the insulating layer is on at least two lateral sides of the conductive layer.

52. The method of claim 51, wherein the insulating layer is formed having a thickness within the range of approximately 20 to approximately 100 Å.

53. The method of claim 51, wherein the act of forming the doped surface layer comprises forming the doped surface layer in contact with the insulating layer.

54. The method of claim 38, wherein the act of forming the gate comprises forming the gate such that operation of the gate affects the doped surface layer at least partially through a sidewall of the gate.

55. A method of forming a pixel cell, the method comprising:

forming a trench in a substrate;

forming a gate of a transistor in the trench;

forming a photo-conversion device adjacent to the gate, the act of forming the photo-conversion device comprising forming a doped surface layer of a first conductivity type, such that the doped surface layer is at a

level at least partially above a level of a bottom surface of the trench, and forming a doped region of a second conductivity type underlying the doped surface region.

56. The method of claim 55, wherein the trench is formed having a depth within the range of approximately 500 to approximately 2500 Å.

57. The method of claim 55, wherein the act of forming the gate comprises:

forming a conductive layer; and

forming an insulating layer, such that the insulating layer is on at least two lateral sides of the conductive layer.

58. The method of claim 57, wherein the insulating layer is formed having a thickness within the range of approximately 20 to approximately 100 Å.